Institution: The University of Edinburgh

Unit of Assessment: B11 — Computer Science and Informatics

Title of case study: The EnCore Microprocessor and the ArcSim Simulator

1. Summary of the impact

This case study describes the impact of the EnCore microprocessor, and the associated ArcSim simulation software, created in 2009 by the *Processor Automated Synthesis by iTerative Analysis* (PASTA) research group under Professor Nigel Topham at the University of Edinburgh. Licensing to Synopsys Inc. in 2012 brought the EnCore and ArcSim technologies to the market. Synopsys Inc. is a world-leading Silicon Valley company. It is the largest Electronic Design Automation (EDA) company in the world, and the second largest supplier of semiconductor IP. EnCore is achieving a global impact through this worldwide channel. The commercial derivatives of the EnCore technology provide manufacturers of consumer electronics devices with an innovative low-power, high-performance microprocessor that they can customize to their specific application requirements, enabling the next generation of electronic devices.

2. Underpinning research

The School of Informatics staff who conducted the underpinning research were Professor Nigel Topham (2003–date), Professor Michael O'Boyle (1997–date) and Dr Björn Franke (Lecturer, then Reader 2003–date) and their students Richard Bennett (PhD, 2011), Igor Böhm (PhD, 2013), Edwin Bonilla (PhD 2008), Tobias Edler von Koch (current PhD student), Alastair Murray (PhD 2012), Karthik T. Sundararajan (current PhD student) and Marcela Zuluaga (PhD, 2010).

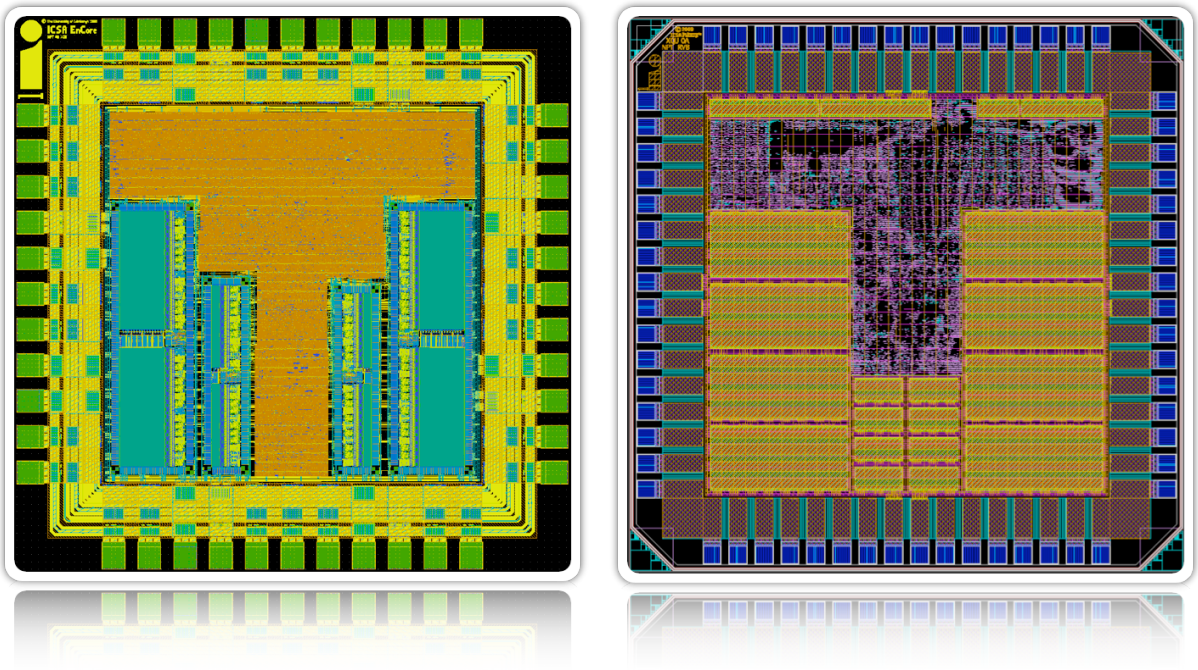
The EPSRC-funded PASTA project (EP/D50399/X1) developed the EnCore microprocessor and the ArcSim simulation software, initially as research prototypes. The PASTA project ran from September 2006 to August 2010. Prof Nigel Topham led the project as principal investigator with Dr Björn Franke and Prof Mike O'Boyle as co-investigators. The focus of the project was to investigate new and novel methods of automating the design of embedded processors. It took a system-wide approach, and thus had a broad remit to consider aspects ranging from low-level hardware implementation, through instruction-set customization, and on to compiler optimization.

Full information is available on the PASTA project website at *http://groups.inf.ed.ac.uk/pasta/*. This website provides additional data on the EnCore processor, including technical details, images and all published papers.

The team took the view from the outset that realistic research into microprocessor synthesis would require an industrial-strength prototype through which to evaluate research innovations. This led to the creation of the EnCore microprocessor, initially as an experimental tool. In 2009 the first EnCore implementation was validated through the fabrication of Calton, a prototype silicon chip. The Calton chip was fabricated in a 130nm UMC process in Taiwan, via Europractice. It was fully functional in its first silicon fabrication.

The PASTA project had several thematic research areas, running parallel through the project, each of which contributed towards the overall impact of the EnCore microprocessor and the ArcSim simulator. Foremost of these was the theme of processor customization; this led to new machine-learning algorithms for predicting design trade-offs [1], to new techniques in design-space exploration [2], and explored the interactions between compiler transformations and instruction-set extension [3]. Research innovations in energy-saving cache architectures were developed [4], and new compiler optimizations were devised for systems where code-density is critical [5].

Figure 1: The Calton and Castle EnCore processors



A key requirement for design-space exploration is the ability to simulate new features of a microprocessor before it is actually implemented. To support this, the PASTA project team developed ArcSim, an ultra high-speed simulation tool [6]. This is arguably the fastest simulator in its class, due to its novel JIT binary translation, and was separately licensed by Synopsys in 2012. Additional information on the ArcSim simulator including video demos is provided on the ArcSim pages on the PASTA project website at *http://groups.inf.ed.ac.uk/pasta/tools_arcsim.html*

The PASTA project culminated in the fabrication of a second silicon chip, Castle, another realisation of the EnCore microprocessor design. The Castle chip incorporated some of the synthetic extensions enabled by the ideas developed in the project, to evaluate their effectiveness in real silicon. It is 4mm square. A 90nm UMC process fabricated the chip, which was fully functional at 600 MHz in its first silicon fabrication.

3. References to the research

1. M. Zuluaga, E. Bonilla and N. Topham, “Predicting Best Design Trade-offs: A Case Study in Processor Customization”, *Proceedings of Design, Automation and Test in Europe* (DATE '12), 2012.

   DOI: *http://doi.ieeecomputersociety.org/10.1109/DATE.2012.6176647*

2. M. Zuluaga and N.P. Topham, “Design Space Exploration of Resource Sharing Solutions for Custom Instruction Set Extensions”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (TCAD'09), volume 28, issue 12, pages 1788-1801, 2009.

   DOI: *http://dx.doi.org/10.1109/TCAD.2009.2026355*

3. A. Murray, R.V. Bennett, B. Franke and N.P. Topham, “Code Transformation and Instruction Set Extensions”, *ACM Transactions on Embedded Computing Systems* (TECS '09), volume 8, issue 4, 2009.

   DOI: *http://dx.doi.org/10.1145/1550987.1550989*

4. K. Sundararajan, V. Porpodas, T. Jones, N. Topham and B. Franke, "Cooperative Partitioning: Energy-Efficient Cache Partitioning for High-Performance CMPs", *Proceedings of the 18th International Symposium on High Performance Computer Architecture* (HPCA'12), New Orleans, 2012.

   DOI: *http://dx.doi.org/10.1109/HPCA.2012.6169036*

5. T. Edler von Koch, I. Böhm and B. Franke, "Integrated Instruction Selection and Register Allocation for Compact Code Generation Exploiting Freeform Mixing of 16- and 32-bit Instructions", *Proceedings of the 8th annual IEEE/ACM International Symposium on Code generation and optimization* (CGO '10), Toronto, Canada, 2010.

   DOI: *http://dx.doi.org/10.1145/1772954.1772980*

6. I. Böhm, T. Edler von Koch, S. Kyle, B. Franke and N. Topham, "Generalized Just-In-Time Trace Compilation using a Parallel Task Farm in a Dynamic Binary Translator", *ACM SIGPLAN 2011 Conference on Programming Language Design and Implementation* (PLDI'11), San Jose, CA, 2011.

   DOI: *http://dx.doi.org/10.1145/1993498.1993508*

Of these, references [2], [5] and [6] are most indicative of the quality of the underpinning research.

4. Details of the impact

The primary route to impact of the PASTA project has been through the commercial licensing of the EnCore and ArcSim technologies by Synopsys Inc [F]. ArcSim was licensed to ARC International PLC in 2007, and through company acquisitions it was acquired by Synopsys. (Synopsys acquired Virage Logic in 2010, including ARC International PLC.) Synopsys re-licensed in 2011, to obtain the latest improved revision of ArcSim. The EnCore license agreement was signed in March 2010, and by October 2011 Synopsys released the first products based on EnCore and ArcSim. These were [text removed for publication], and the nSIM simulator [E].

Embedded processors are at the heart of all smart electronic devices, in markets such as mobile phones, data centres and networking, computing and peripherals, medical appliances, automotive electronics, avionics and the digital home. Manufacturers of these electronic devices typically license the design of an embedded processor as an intellectual property (IP) core.

Manufacturers worldwide produced over 10 billion chips containing an embedded IP processor in the 2011 financial year [A, B]. The ARC processor cores from Synopsys were the second largest in volume, accounting for 10% of that market. By volume, this places them below ARM, but above MIPS, Imagination, Ceva and Tensilica (their main competitors). This market is growing at 10% annually. Synopsys' overall revenues for the 2011 financial year were $1.54B. This is an increase of 11% on the previous year [A]. This serves to demonstrate (a) the size of the market in which EnCore will have an impact, and (b) the world-leading presence of Synopsys, as a force through which EnCore is already creating an impact.

The wider commercial deployment of the EnCore design is resulting in the dissemination into everyday electronic devices of its advanced features for low-power, small silicon area, and high performance. This will provide greater functionality, at lower cost to the end-user, while consuming less energy [C]. Hence, mobile or battery-powered devices will see extended lifetimes. The compact dimensions of an EnCore processor will enable larger numbers of processors to be integrated within the same chip, enabling wider deployment of many-core systems, which in turn will enable new system-level functionalities.

We believe that sustained engagement and impact will only continue in the longer term if both

academic and industrial partners receive benefits from continued cooperation. The University of Edinburgh is benefitting financially through its licensing agreements and in turn this is feeding through to support future research in processor design and related areas. Within the Institute for Computing Systems Architecture in the School of Informatics several PhD scholarships have already been funded internally through EnCore licensing revenues. These revenues from licensing are pooled with our research institute finances to facilitate funding of PhD students.

A further benefit of the EnCore development within Edinburgh University is the creation of a nationally important capability in microprocessor design. EnCore is a unique example of a UK university research group designing a microprocessor and then licensing it to an industry partner who is capable of marketing it on a truly worldwide scale. The technology is now in a prime position in the market and experiencing take-up.

5. Sources to corroborate the impact

A. Synopsys Annual Financial Statement, 2011:
http://www.synopsys.com/company/locations/armenia/news/pages/pressid11302011.aspx
Provided to back up claims regarding recent financial status of the licensee.

B. Rick Merrit, "ARM Dominates 10B unit CPU core market": EE Times online, 5th October 2012, *http://eetimes.com/electronics-news/4372693*

C. EPSRC: "New Microprocessor Could Extend Battery Life", Case Study 25,
http://www.epsrc.ac.uk/newsevents/casestudies/2009/Pages/newmicroprocessor.aspx
Issue date 07 July 2009. Print version:
http://www.epsrc.ac.uk/SiteCollectionDocuments/Publications/casestudies/IMPACTCaseStudy25MicroprocessorExtendBatteryLife.pdf
The Engineering and Physical Sciences Research Council commissioned this article to highlight the impact of the PASTA project, which they funded.

D. [Text removed for publication]

E. Synopsys, product landing page for the nSIM simulator:
http://www.synopsys.com/dw/ipdir.php?ds=sim_nsim
Contains an online overview of technical details of the nSIM simulator, which is derived from the ArcSim technology, licensed by the University of Edinburgh to Synopsys Inc.

F. Vice President Engineering, Solutions Group at Synopsys, Inc.
This source represents the licensing group within Synopsys and can be approached for a reference if required to corroborate details about the license.

Archive copies of these webpages are available from *http://ref2014.inf.ed.ac.uk/impact/*