Institution: University of Surrey

Unit of Assessment: UOA 13 Electrical and Electronic Engineering, Metallurgy and Materials

Title of case study: Surrey NanoSystems

Meeting the International Technology Roadmap for Semiconductors

1. Summary of the impact (indicative maximum 100 words)

Surrey Spin-out Surrey Nano Systems (SNS) is a business based around key patents resulting from the work of Prof. Ravi Silva and his team. SNS has raised over £11M from investors who have scrutinised the technology and recognise its value. The business develops technologies for low-substrate-temperature growth of carbon nanotubes (CNTs) and for novel low-*k* dielectric materials both of which align with the International Technology Roadmap for Semiconductors (ITRS). SNS is working closely with multinational leaders and has attracted a team that includes senior management experience of selling into the semiconductor process equipment market.

2. Underpinning research (indicative maximum 500 words)

In a highly-interactive, multi-disciplinary research environment there is rarely a simple, linear relationship between a single research programme and a high-impact outcome. In this case, the primary initiating research was a MOD contract placed through BAe Systems (Sowerby, Bristol) in 1997/8. Surrey's research team (led by Prof. Silva) were carrying out research on stealth materials and high emissivity surfaces. This led to the development of new techniques for the production of thin-film carbon coatings [1].

The key inventive step was that the team recognised that the use of heating from above the substrate together with an engineered surface layer allowed high temperature carbon CVD growth processes with the bulk substrate kept at low temperature [2-5]. This recognition resulted from previous experience in rapid thermal annealing process development, with the heat being delivered by an array of halogen lamps. This process is now known as Photo-Thermal Chemical Vapour Deposition (PTCVD) [3,5].

It was apparent that this new technique could address a key challenge in the application of carbon nanotubes in the production of integrated circuits, specifically in advanced CMOS. Carbon nanotubes (CNTs) have well-understood advantages, particularly as interlayer vias, but were not hitherto grown at sufficient quality at process temperatures that CMOS devices can withstand.

In the course of developing the CNT growth process it was discovered that a new polymer material could be deposited using the same essential CVD process. This polymer was found to have very low dielectric constant, capable of meeting a further need of the advanced CMOS industry [6].

The research work (2001-5) has resulted in the filing of multiple patents, often in conjunction with industrial collaborators. Subsequent to patent filings, papers were published in high impact journals including Nature Materials [3,5].

Recognising the significant commercial potential of both aspects of this work the team partnered with the then Regional Development Agency SEEDA to spin-out these elements of the research through the formation of Surrey NanoSystems Ltd (2008). Research activity has continued to support this spin-out business. SNS initially operated as a supplier of PTCVD and allied growth equipment to the global research community. Following second-round venture funding the business re-aligned to the exploitation of the process knowledge directly to semiconductor majors.

Further research themes have developed from this work. Current commercially-funded activity includes the development of a moisture-barrier coating, initially for satellite components, but having potential for future application in encapsulation of organic semiconductor devices. The PTCVD process is expected to have important future application in the formation of graphene layers, with the halogen lamps being replaced with high-power LEDs to allow the more rapid modulation of the power.

The Surrey research team was led by Prof R.Silva included G.Y.Chen, B.O.Boskovic, S.Haq and V.Stolojan

3. References to the research (indicative maximum of six references)

1. High Emissivity Radiator patent number US7812327, filing date Sept. 30 (2005), Inventors: Sajad Haq, Michael Christopher Hebbron, José Virgilio Anguita Rodriguez, Sembukuttiarachilage Ravi Pradip Silva.
2. Production of carbon nanotubes patent application number 10/484,894, US 2004/0253167 A1, Filing date: Aug 4, 2004. Inventors: Sembukutiarachilage Ravi Silva, Sajad Haq, Bojan O. Boskovic.
3. B.O. Boskovic, V. Stolojan, R.U.A. Khan, S. Haq, S.R.P. Silva, "Large Area Synsthesis of Carbon Nanofibres at Room temperature", Nature Materials, **1,** (2002) 165-168.
4. Nanostructure production methods and apparatus with patent application number 11/920,280, US 2009/0061217 A1, filing date: May 11, 2006. Inventors: Sembukutiarachilage Ravi Silva, Ben Paul Jensen, Guan Yow Chen.
5. G.Y. Chen, B. Jensen, V. Stolojan, S.R.P. Silva, "Growth of carbon nanotubes at temperatures compatible with integrated circuit technologies", CARBON, 49 (1) (2011) 280-285. doi: 10.1016/j.carbon.2010.09.021
6. Material having a low dielectric constant and method of making the same patent application number 13/264,885, US 2012/0043640 A1, Filing date: Apr 16, 2010. Inventors: Sembukuttiarachilage Ravi Pradip Silva, José Virgilio Anguita Rodriguez Estefania.

4. Details of the impact (indicative maximum 750 words)

The impact that our research has had can be demonstrated in the commercial application (described at the end of this section) but also in the recognition received:

- a Chairman's award from BAE Systems;
- Surrey was awarded a commercialisation award for £250k from SEEDA;
- SNS received a £750k investment from IP Group;
- SNS equipment sales of £1.5M per annum to the global research community during the start-up phase alone.

The semiconductor industry, whose worth is measured in billions of dollars, urgently needs new interconnection technology and low-k dielectrics to maintain the pace of innovation according to Moore's law. The limitations of existing manufacturing technology threaten the evolution to next-generation geometry sizes, speeds and power conservation.

Manufacturers in the semiconductor industry, currently use copper to provide the vertical interconnections required for integrated circuit (IC) fabrication. Carbon Nanotubes (CNT) can be structured to act as extremely efficient conductors, but their adoption as a replacement for copper has been hindered by the fact that conventionally grown CNTs require temperatures of around 700 degrees centigrade. This is too high for semiconductor processing, and leads to the destruction of the microchip circuitry. In parallel, the semiconductor industry has continuing needs for better dielectric materials. In this context, better means lower dielectric constant with solid materials preferred over highly porous systems. The materials processes must integrate smoothly with the remaining processes as the technology need is for an incremental change rather than a disruptive re-engineering.

"SNS's low-k material offers a potential step-change for dielectrics with a k value that meets the requirements of 22 nm integrated circuit technology"
Chair of ITRS Interconnect Working Group

These two, well-understood industry needs are the primary target market for Surrey NanoSystems Ltd. The highly innovative PTCVD process, which provides the ability to grow carbon nanomaterials at low substrate temperatures, is the technology that underpins SNS. It removes a major obstacle in using devices such as CNT in next generation microchip manufacture. SNS was formed in 2008 to commercialise the technology and has developed it into the world's first "turn-key" NanoGrowth^{TM} machine for the cost-effective, low-temperature production of precision aligned multi-wall carbon nanomaterials. The commercial development is entirely focussed on meeting the International Technology Roadmap for Semiconductors (ITRS). This is a high-risk, high-reward strategy and is supported by venture capital.

"…..we would consider a film with these verified novel characteristics as interesting, and would therefore be interested in further internal evaluation for suitability of potential use [in a manufacturing process] in the future…..".
Manager, Intel Ireland

The NanoGrowth^{TM} machine, provides a fabrication system that allows CNT structures and low-k dielectrics to be grown at silicon friendly processing temperatures, that is below 450 degrees C, making viable a new interconnection process for high-volume semiconductor manufacture. This is the first commercially available nanomaterial growth machine that allows the user to easily and precisely control the rapid growth, quality and characteristics of carbon nanotubes and low-k dielectrics using fully tested "ingredient mix recipes."

SNS was formed in 2008. The first stage of the business model was based on developing the market for the NanoGrowth^{TM} machine in academic and commercial research laboratories. As a result of this strategy, many research establishments around the world have entered into partnership agreements with SNS. The second part of the business plan was to attract further investment and to incorporate the technology more widely into a range of manufacturing processes. This is now underway, following the £4.5m of 2nd round funding that was recently (2012) secured. The company's base is in Newhaven, and has already hired 20 staff to run the activities. Dr G.Y.Chen has transferred from the University of Surrey as CTO and Prof Silva is CSO and a Board member together with K.Robson from Surrey's Research and Enterprise Support office. The new business is still growing, but has already impacted considerably in the area in terms of providing employment and economic regeneration.

SNS expects the overall market to grow at approximately 10% per year and notes that downturns in the sector often see increased spend in R&D. The key part of the market to SNS is the semiconductor wafer fab equipment, worth approx. $33bn in 2008 and expected to grow to $41bn by 2012. The low-k materials market in itself was worth over $2.4bn in 2011, and together with the interconnect market unlocks the $250bn semiconductor industry IC manufacturers and equipment vendors. SNS has started the validation process for their equipment to be incorporated in the 2014 IC cycle which has a 2 year lead time.

5. Sources to corroborate the impact (indicative maximum of 10 references)

C1. CEO Surrey NanoSystems. Contact details provided.

C2. Former Chairman, Surrey NanoSystems. Contact details provided.

C3. Commercialisation potential: IP Group Chairman. Contact details provided.

C4. ITRS Technology Roadmap Interconnect Working Group http://www.itrs.net/ITWG/models.html

C5. World expert in CMOS and industry outlook, Manager at INTEL Ireland. Contact details provided.

C6. Start-Up and University Collaboration category at the Engineer Technology and Innovation Awards organised by The Engineer magazine, 2007.

C7. Most Entrepreneurial Scientist in the UK, Runners-up, UKSECs the national network of Enterprise Centres, and Science Alliance, 2006.

C8. Won BAE Chairman's Award in 2004 for Innovations and Implementation (Room temperature growth of Carbon nanotubes: Dr. Sajad Haq (Haq, Sajad (UK) [Sajad.Haq@baesystems.com]), Prof. Ravi Silva)

C9. IEE Innovations in Engineering Award in Emerging Technologies 2005 for Innovations and Contributions to nanotechnology (Prof. Ravi Silva, University of Surrey)

C10. Shortlisted for ACES- Academic Enterprise Awards - Europe 2010. Runners up in Materials and Chemistry category 2009.