Institution: University of Glasgow
Unit of Assessment: B15: General Engineering
Title of case study: **Unique simulation software tools for the global semiconductor industry**
1. Summary of the impact

The development of unique computer simulation tools has profoundly influenced the design and manufacture of silicon chips fuelling the $300 billion per year semiconductor industry. A pioneer of statistical variability research, Professor Asen Asenov developed understanding and awareness of statistical variability in the nanoscale transistors which make up all silicon chips. Gold Standard Simulations (GSS) was created in 2010 and by 2012-13 had grown revenue from services and licensing to $1million. GSS tools are currently used in foundries providing 75% of all semiconductor production for fabless design companies globally. For example, working with GSS and their simulation tools has reduced the development time for IBM's next generation of CMOS technology by 1 year, representing significant savings in the 3-5 year technology development cycle.

2. Underpinning research

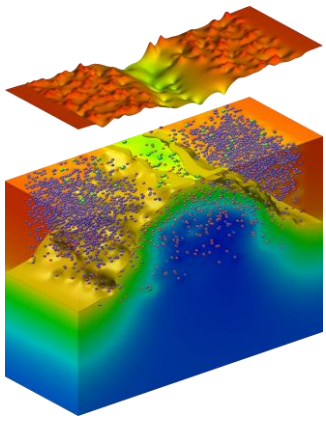

Figure 1. GSS simulation.

The demand for ever more powerful silicon chips has driven continued miniaturisation of transistors. However, the performance of these devices is increasingly affected by atomic imperfections in their structure as they reduce in size. Known as the 'Christmas pudding effect', it is impossible to predict how many dopants, introduced randomly, will end up in each nanoscale transistor. Dopants are like raisins in the Christmas pudding – each portion (transistor) has a different number of raisins (dopants). This problem critically affects the yield of static random-access memory (SRAM), introduces timing issues in digital circuits, restricting supply voltage scaling and increases the power dissipation. SRAM occupies more than 50% of modern silicon chips used in computers, smartphones and tablets.

Numerical simulations play a key role in understanding statistical variability of Complementary Metal-Oxide-Semiconductor (CMOS) and in predicting its impact on future technology generations, with a single chip containing billions of transistors. CMOS is a technology for constructing integrated circuits. Professor Asen Asenov (James Watt Chair in Electrical Engineering, School of Engineering, 1991-present) was the first person in the world to research systematically statistical variability in CMOS transistors and since 1998 has secured over £11million in research funding to focus on the development of a unique variability simulation toolchain. This research developed a significant body of work, including IP in the form of software that led to the formation of spin-out Gold Standard Simulations (GSS) in 2010.

In 1998, Asenov was approached by NASA, who recognised the problem of randomness of dopants within transistors. Facilitated by Henry MacDonald (Director of NASA's Ames Research Center) Asenov and Dr Andrew Brown (Research Assistant (RA), 1998-2010) were funded to develop tools for parallel finite element simulation of 'atomistic' effects in sub-0.1micron transistors. The first version of the simulation software was able to resolve atomic scale effects in nano-CMOS transistors [1]. Scottish Higher Education Funding Council support continued to support the research (VIDEOS 1999-2002).

Asenov's Device Modelling Research Group developed 'atomistic' Monte Carlo and NEGF (non-equilibrium Greens function) Quantum Transport simulators for nano-CMOS devices, capable of modelling all known sources of intrinsic parameter variations [2-6]. In recognition of Asenov's work,

IBM awarded him the prestigious $1 million Shared University Research Award 'Investigating Intrinsic Fluctuations in Decanano Silicon Devices' (2001-04). This helped to determine the impact on scaling, device architecture and circuit performance [4].

Asenov and Binjie Cheng (RA 2002-present) revealed that the variability within transistors could be quantified and actually utilised in neural networks to allow efficient training in pattern recognition (EPSRC GR/R47325/01 2001-05). University College London's expertise in first principle material simulations was brought in to gain a deeper understanding of how device atomic structure impacts on the behaviour of transistors; they provided atomic-scale material simulations, the methods for which were transferred into Glasgow's device-level simulation code (EPSRC 2004-08, GR/S80097/01). The development of the tools was also supported by consecutive EPSRC Platform grants (2003-2007, GR/R89738/01, 2007-2013, EP/E038344/1).

FP6 PULL NANO (2006-08) focused on the development of 32nm technologies in Europe. Collaborators ST Microelectronics, Infineon and NXP provided experimental data which facilitated the validation and calibration of the device simulation tools. The expertise in physical simulation was translated into compact models (EPSRC EP/E003125/1, 2006-2010). Asenov, with Professor Scott Roy (Lecturer 1994-2012, Professor of Electronics 2012-present), Dr Campbell Millar (RA 2003-09) and the Universities of Edinburgh (Prof A. Murray, School of Engineering), Southampton (Prof M. Zwolinski, Dept of Electronics and Computer Science), York (Prof A Tyrrell, Dept of Electronics) and Manchester (Prof S. B. Furber, Dept of Computing Science), developed a new toolset including compact model extraction and circuit simulations. The resulting software is at the core of the GSS simulation toolchain. Subsequent FP7 funding allowed researchers to focus on how statistical variability impacts on design (REALITY 2008-10). Using industrial data from ST Microelectronics, the predictive capabilities and accuracy of the tools were demonstrated. The toolchain allows the generic optimisation of SRAM.

Further research and commercially focused development were carried out through the EU Electronic Numerical Integrator And Computer (ENIAC) project MODERN (2009-12). During this project GSS was formed to commercially deliver simulation tools to the ENIAC partners. Collaborative EU projects have been important in the ongoing University research and the development of the GSS tools. Working with key industry partners, the tools have been applied to new applications:

- TRAMS (2010-13) with Intel where University/GSS technology was used for first time to simulate FinFETs (multi-gate or tri-gate architectures);
- MOERDRED (2010-14) with Infinion where statistical reliability was introduced in the University/GSS tools;
- SUPERTHEME (2012-15) with Austria Microsytems (AMS) where the University/GSS technology has been adopted for analogue design.

3. References to the research

1. A. Asenov, Random dopant induced threshold voltage lowering and fluctuations in sub 0.1 micron MOSFETs: A 3D 'atomistic' simulation study, *IEEE Transactions on Electron Devices*, vol. 45, no. 12, pp 2505-2513 (1998). (doi:10.1109/16.735728). Single authored paper cited 415 times (average number of citations in the field 2). The relevance of the paper is increasing with time according to the yearly citation count. *
2. A. Asenov, A. R. Brown J. H. Davies, S. Kaya†, and G. Slavcheva, Simulation of Intrinsic Parameter Fluctuations in Decananometre and Nanometre scale MOSFETs, *IEEE Transactions on Electron Devices,* vol. 50, pp. 1837-1852 (2003). (doi:10.1109/TED.2003.815862). Invited paper 367 citations. *
3. A. Asenov, S. Kaya and A. R. Brown, Intrinsic Parameter Fluctuations in Decananometre MOSFETs Introduced by Gate Line Edge Roughness, *IEEE Transactions on Electron Devices*, vol. 50, pp. 1254-1260 (2003). (doi:10.1109/TED.2003.813457). 307 citations. *

4. G. Roy, A. R. Brown, F. Adamu-Lema, S. Roy and A. Asenov, Simulation Study of Individual and Combined Sources of Intrinsic Parameter Fluctuations in Conventional Nano-MOSFETs, *IEEE Transactions on Electron Devices,* vol. 52, pp. 3063-3070 (2006). (doi:10.1109/TED.2006.885683). 167 citations.

5. A. Asenov, G. Slavcheva, A.R. Brown, J.H. Davies and S. Saini, Increase in the random dopant induced threshold fluctuations and lowering in sub-100 nm MOSFETs due to quantum effects: A 3-D density-gradient simulation study, *IEEE Transactions on Electron Devices*, vol. 48, pp. 722-729, (2001). (doi:10.1109/16.915703). 200 citations.

6. A. Asenov, S. Kaya, J. H. Davies, Intrinsic Threshold Voltage Fluctuations in Decanano MOSFETs due to Local Oxide Thickness Variations, *IEEE Transactions on Electron Devices*, vol. 49, pp. 112-119 (2002). (doi:10.1109/16.974757). 153 citations.

* best indicators of research quality

4. Details of the impact

Pioneering research led by Asenov and the Device Modelling Group has had major impacts on the global semiconductor industry by (i) developing understanding and awareness of the challenge of statistical variability; and (ii) providing economic impacts through the development of a novel software toolchain commercialised through spin-out company Gold Standard Simulations.

Developing understanding and awareness of the challenge of statistical variability
When Asenov first discussed the issue of statistical variability with the global semiconductor industry in the late 1990s, it was generally believed that transistors were sufficiently large that this would not affect performance. However, the drive for miniaturisation of semiconductor devices has revealed that statistical variability is absolutely critical to the performance of silicon chips. Asenov was the first to systematically explore the problem of statistical variability and the ramifications for the world's electronics industry. His findings and opinions expressed through invited talks at international conferences (66 appearances since 2008), training courses run in Silicon Valley, key professional journals and the media have shaped understanding and awareness and have influenced practices in the $300 billion per year semiconductor industry.

Providing economic impacts through the development of a novel software toolchain
Asenov's Device Modelling Group developed one of the first integrated simulators of variability for Complementary Metal-Oxide-Semiconductor (CMOS) devices and processes, building a unique variability simulation software toolchain. From 2007-12 Asenov's EPSRC funded research was closely aligned to industry demands (collaborators included key figures in the semiconductor industry, such as STMicroelectronics, Infineon and NXP). Working with Synopsis Inc he developed interfaces for the Glasgow simulation tools.

Asenov and Millar joined **Gold Standard Simulations** (GSS) as CEO and COO when it was spun out of the University of Glasgow in 2010 with support from Scottish Enterprise and EPSRC. The EU Electronic Numerical Integrator And Computer (ENIAC) project 'Modelling and Design of Reliable process variation-aware nanoelectronic devices, circuits and systems' (2009-12) was the catalyst for the formation GSS as a vehicle to commercially deliver simulation tools to ENIAC partners. GSS is the first and only company to provide a fully integrated service and toolchain allowing device/circuit co-design and assessment of contemporary and future CMOS technology options. GSS employs 8 people and in 2012-13 secured $1m in revenue. GSS have licenced their tools to major foundries and have evaluation licences in place with others.

In 2010 IBM engaged with GSS to investigate the 'shape' of the next FinFET (14nm) generation CMOS technology. A Senior Researcher at IBM stated:

> "*GSS and University researchers developed a range of memory device scenarios, promptly rejecting low yield designs, and avoiding the time and expense of trying numerous memory topologies in hardware. This project saved at least one year in the memory development process, which is quite a significant part of the 3-5 year technology development cycle. The results of the pathfinding work that IBM has done with GSS will naturally be shared with and*

directly benefit IBM's technology platform partners like Samsung and Global Foundries. Globally investment in semiconductor R&D is reducing so it is important that Prof. Asenov continues to blaze a trail to allow the few companies moving forward to the next semiconductor node to be able to continue their efforts. The biggest indicator of the benefits of the GSS expertise and tools is that IBM is undertaking an assessment of the tools with a view to licensing the GSS technology."

The GSS expertise and toolset is allowing integrated device manufacturers, foundries and fabless design companies across Europe, the Far East and the USA to gain significant competitive advantage over their competitors by reducing time to market, avoiding overdesign, increasing yield and de-risking the expensive chip design process. GSS tools provide designers with the benefit of 'seeing into the future' to determine which circuits will work optimally in new devices, thus eliminating the expense of fabricating in silicon at the design stage. Time savings equate to significant cost saving given that recent estimates state that the next generation of semiconductors will cost $10-20bn to create.

GSS have also supported the development of Yorkshire based start-up SureCore Ltd, providing crucial knowledge and training on statistical variability. SureCore successfully combined their own circuit and system design knowledge with the device modelling expertise of GSS. SureCore's partnership with GSS has enabled the company to develop variability tolerant SRAM, resulting in leading edge memory solutions that consume less than half the power of comparable memories – key to reducing battery requirements for mobile devices. GSS have strengthened SureCore's credibility within the market and enabled them to substantially develop their business. In 2013 a University of York spin-out, Ngenics, also licenced the GSS tools to strengthen their business.

5. Sources to corroborate the impact

- Statement from VP Business Development, Gold Standard Simulations Ltd. (on role of the University of Glasgow in the formation of GSS)
- Senior Technical Staff, IBM (on impact of University of Glasgow and GSS tools on IBM R&D) (contact details and statement provided)
- CEO, SureCore Ltd (on role of GSS in development of SureCore) (contact details provided)

Media Coverage (demonstrating University of Glasgow led industry awareness and dialogue):

- Planet Analog Website: Prof Asenov writes about the importance of statistical variability 'CMOS statistical variability: The skeleton in the closet'. 14/04/09
- New Electronics website: (The Site for Electronic Design Engineers) Prof Asenov highlights the importance of variability to CMOS technology - 'CMOS' future depends on statistics', 9/8/10
- BBC News website: 'Grid computing tunes BBC News website: Prof Asenov quoted on simulation of transistors 'Grid computing tunes tiny transistors for future chips', 4/12/09
- EE Times website (Connecting the Global Electronics Community): Article highlighting GSS simulation service to chip developers and manufacturers. 'Startup offers 'variability' modeling service', 2/09/10
- Electronics Weekly.com article: 'GSS tackles CMOS statistical variability', 28/07/11
- EE Times website: Prof Asenov comments on Intel FinFet technology based on GSS simulations. 'Intel's FinFETs are less fin and more triangle', 17/05/12