Institution: Queen's University Belfast

Unit of Assessment: 13

Title of case study: System-on-Chip (SoC) IP cores for Digital TV and multi-media systems

1. Summary of the impact

Research (1993-2008) on novel silicon architectures and design methodologies for digital signal and video processing led to the creation of world leading semiconductor IP cores (chip designs) for implementing the main video and image compression standards including H.264, MPEG4, MPEG2, and JPEG2000. These have been licensed to semiconductor manufacturers worldwide including Panasonic, Sony, Toshiba and Sharp. Since 2008, such encoders/decoders have been incorporated into all DTV/HDTV SoCs produced by Conexant, NXP, Trident Microsystems and Entropic. They have also been used as the hardware acceleration engines in Intel's C2110 Media Processor. At least 150 million chips worldwide having been manufactured incorporating this technology.

2. Underpinning research

Researchers involved *Professor John McCanny(1993-), Dr Yi Hu (1993-96, PDRA), Dr T J Ding (1993-1999, PhD then PDRA), Dr Maire O'Neill (nee McLoone, 1999-2002 PhD, 2003-2008, RAEng Research Fellow), Dr S Y Yap (2000-2004, PhD), Dr Jill Hunter (1995-1999, PhD), Dr Shahid Masud (1995-1999 PhD, Dr J Sun (1998-2002, PDRA).*
Hu, Hunter, Masud and Sun were subsequently employed by Amphion Semiconductor Ltd.; Hu later became Amphion's Chief Technologist. O'Neill is now a Professor in the UoA.

Time period, 1993-2004

By the early nineties it was possible to fabricate silicon chips with hundreds of millions of transistors. This coincided with an insatiable demand for real-time computational rates driven by emerging applications such as multi-media systems and HDTV. This created a number of major challenges. The first was to create novel silicon architectures that could meet the very demanding real-time computational rates required in a highly cost effective manner (i.e. small silicon footprint and low power dissipation). Far beyond the capabilities of then available microprocessor solutions. The second was to address the challenges of correctly designing chips of this complexity. This led to a number of inter-related research programmes, an important outcome of which was the creation of new silicon computational architectures and methods for the design of complex signal and video processing chips. These exploited the inherently regular architectures that typify datapaths for implementing DSP functions such as filters, transforms, convolutional decoders etc. and built on our pioneering research in this field (partly summarised in [1]). A key observation was to note that, whilst new DSP/video processing algorithms are continually being created, these typically decompose into a finite set of sub-computations such as FFTs, DCTs, Wavelet transforms, digital filters etc., albeit with different transform sizes, filter lengths, word lengths and data flows. This led to the creation of libraries of parameterised architectural templates captured in the VHDL hardware description language [2].

Initially this was done for building blocks such as fixed and floating point arithmetic processors. These were then used to build many different and parameterisable variants of circuits for implementing FIR filters, FFT and DCT processors etc. and in turn to create more complex systems, examples being families of video decoders and encoders for standards such as H.264, MPEG4 and MPEG2, JPEG2000 and JPEG. The use of scripts allowed highly optimised, synthesisable designs to be created at the lower levels. This hierarchical approach ensured efficiencies were maintained through higher levels of complexity. Thus, very highly competitive chip designs – measured in terms of performance, gate count and power dissipation- could be, and were created *in a fraction of the time previously thought possible* – days and weeks rather than months and years [2-5] which, using design synthesis methods, could be mapped directly onto

more advanced silicon fabrication processes as these emerged. Related research resulted in novel computational methods and architectures [6] for variable block size motion estimation - extensively used in modern video standards. This showed how the 41 sub-block motion vectors typically required can be computed in the same number of clock cycles as were needed previously for one motion vector.

3. References to the research

Six publications covering/underpinning this research are listed below. These have undergone rigorous peer review and the research funded through the externally peer-reviewed external grants shown. The three highlighted papers* are selected as being indicative of the quality underpinning the research.

1. Woods RF, McCanny JV, McWhirter JG, 'From Bit Level Systolic Arrays to HDTV Processor Chips', Invited overview paper, Journal of Signal Processing Systems for Signal, Image and Video Technology, Springer, New York, Vol. 53, Numbers 1-2, Nov. 2008 pp35-49, ISSN 193908018 (Print), 10939 -8115 DOI 10.1007/s11265-007-0132-z

*2. McCanny JV, Ridge D, Hu Y, Hunter J, 'Hierarchical VHDL Libraries for DSP ASIC Design', Proc. of the IEEE Intl. Conf. on Acoustics Speech and Signal Processing, Munich, April 1997, pp 675-678, 10.1109/ICASSP.1997.599858.

ICASSP is the IEEE signal processing society's premier international conference. It attracts over 2000 people annually and is attended by the key people in the field, is where all the IEEE Committees meet and where the IEEE Signal Processing Society's annual awards are presented including Fellow elections. This paper currently has 37 Google Scholar citations.

3. Hunter J, McCanny JV, Hu Y and Simpson A, 'JPEG encoder System-on-a-Chip demonstrator', Proc. 33rd IEEE Computer Society Asilomar Conference on Signals, Systems and Computers, Monterey, USA, Nov. 1999, invited paper, Vol.1 pp762-766, DOI 10.1109/ACSSC.1999.832431

*4. Ding TJ, McCanny JV and Hu Yi, 'Rapid Design of Application Specific FFT cores' IEEE Transactions on Signal Processing" Vol. 47, No. 5,pp1371-1381, May 1999, DOI 10.1109/78.757224

This is the main IEEE signal processing journal. This paper currently has 18 Google Scholar citations.

5. Masud S, and McCanny JV, 'Reusable Silicon IP Cores for Discrete Wavelet Transform Applications', IEEE Transactions on Circuits and Systems, Part 1, Fundamental Theory and applications Vol. 51, No. 6, June 2004, pp 1114 –1124 **ISSN:** 15580806, DOI 10.1109/TCSI.2004.829236

*6. Yap SY and McCanny JV, 'A VLSI architecture for variable block size video motion estimation'**,** IEEE Trans. On Circuits and Systems –II Vol**.** 51 Issue**:** 7 pp 384-389, July 2004, DOI 10.1109/TCSII.2004.829555

This is the top IEEE Journal for Circuits and Systems (at that time Circuits and Systems 1 was focused on Fundamental Theory and Applications and IEEE Trans Circuits and Systems II on Analog and Digital Signal Processing Circuits). This paper currently has 165 citations.

Research Grant funding

UoA Academics Professor John McCanny (PI),
RA Dr Tiong Jiu Ding
UoA Funding EPSRC GR/K62941/01 "Synthesis of Application Specific DSP chips using System Level Silicon Algorithms", Dec 1995 to Feb 1999, £135K (pre-FEC), under the Realising our

Potential scheme (ROPA)

UoA Academics Professor John McCanny (PI)
RAs Dr J Sun, **PhD Students** Jill Hunter, Shahid Masud, Maire O'Neill
UoA Funding Industrial Research and Technology Unit (IRTU, now part of InvestNI) "Centres of Excellence" Technology Development Programme funded through EU structural funds – "DSiP Laboratories", 1997- 2002, £1.2M (pre-FEC), established to undertake research into new methods for the rapid design and prototyping of advanced silicon integrated circuits for digital signal and video processing applications.

4. Details of the impact

The research described led to the founding by McCanny (then CTO) of Amphion Semiconductor Ltd. (originally Integrated Silicon Systems Ltd). Amphion rapidly became a world leader in the licensing of semiconductor IP (SIP) for Digital Communications and Digital Video applications. Amphion raised over $15M (1999, 2000, and 2002) in a series of venture-funded rounds led by APAX partners, London. Its workforce grew to around 50 people, including numerous PhDs recruited from the UoA's research labs[1]. One of these, Dr Yi Hu, went on to become Amphion's Chief Silicon Architect/Chief Technologist. The company's major customers included Intel, Toshiba, Microsoft, Broadcom, Hitachi, Panasonic, NEC, Sony, Alcatel, Ericson, Siemens and Mitsubishi. It also built strong strategic partnerships with FPGA companies Xilinx and Altera.

Amphion's SIP Platforms included Wireless LAN baseband processors (IEEE 802.11A, HIPERLAN) and DVB subsystems for Cable, Satellite and Terrestrial DTV. Its video and imaging cores covered encoding and decoding solutions for JPEG, JPEG2000, MPEG2, MPEG4 and H.264. Lower level cores included 2D Wavelet Processors, parameterisable FFTs, FIR and IIR filters and Reed-Solomon and Viterbi decoders for Digital Video Broadcast[2]. These were available for both ASIC and FPGA implementations and exhibited performance levels which in terms of gate count and power consumption were - and continue to be - world state-of-the-art, as they are migrated onto new generations of fabrication technologies.

Amphion was acquired by Conexant Inc in 2004 for $25M. Subsequently, Conexant's STB operations (including its Amphion division) were acquired by NXP Semiconductors (Phillips) in April 2008 NXPAmphion. In February 2010, Trident Microsystems signed an agreement to acquire NXP's television and STB business lines with NXP taking shares in this new venture NXPTrident. Subsequently another STB SoC company, Entropic Communications Inc., (EntropicTrident) acquired the STB assets from Trident Microsystems, including the Belfast-based (former Amphion) video codec team.

The impact of this research and the technology includes the following[3]:

- Since Amphion's acquisition, the same core team has produced the video codec IP for every STB and DTV SoC produced by each of the company's subsequent owners. During the REF period eight such products have been launched with total sales of around fifty million units.

- 2010 - Amphion's decoder cores were incorporated into the Fusion DTV SoC (40nm). This includes the Malone multi-format multi-stream decoder which incorporates 12 different video formats that are now needed due to increasing internet delivery of DTV video. These are also used in the Windsor multi-format (H.264, MPEG2, MPEG4) encoder which was the first silicon deployment of this type of encoder and aimed mainly at Skype video chat on TV, see FusionSoC and FusionHDTVSoc.

- 2011 – More than 100 million STB chipsets incorporating the Amphion video decoder cores were reported to have been shipped worldwide. It is estimated that one third of all HDTV STBs in the world currently use chipsets incorporating Amphion's video decoder cores (H.264, MPEG4, MPEG2). See STBchipsets

- 2011 - Amphion's H.264, MPEG2, MPEG4, AC1 were licensed by Intel and used as the hardware acceleration engines in Intel C2110 Media Processors – see IntelC2110 and C2110architecture . While the numbers of the chips fabricated is not available, the royalties now exceed $10M.

- Amphion's video decoders displaced the NXP/Phillips Tri-media processor in the NXP chipsets used in their STB and DTV applications due to much superior performance in dealing with very demanding video test streams and also because of much lower power dissipation and packing costs. In 2008 these cores were also incorporated into the NXP TV550 DTV SoC – the world's first single chip DTV decoder. This is currently used as the main DTV SoC by Philips, Vizio and by many others, see NXPDTV

- 2011-2012 Amphion's Malone decoder and Windsor encoder IP are now included in Entropic's range of 40nm STB SoCs aimed at the satellite, cable and IPTV markets.

- 2013 - Amphion IP has been taped out into the first of Entropic's new range of cost effective STB SoCs (code named Kore3) and is also being designed into the first of a range of 28nm based STB SoCs, the first of which will include the emerging HEVC/H.265 video codec standards. This is one of the first available on the market supporting this new codec standard.

5. Sources to corroborate the impact

[1]Former Chairman Amphion Semiconductor Ltd.

[2]For Amphion's earlier licensing contracts in Japan contact agent

[3]Design Centre Manager Entropic

Other statements and press releases in support of the above statements can be found at (a) H.264solutions and (b) NXPnews. *A summary of some of the original Amphion cores can be obtained at (a)* Amphioncores, (b) DES/3DES (c) amphion-accelerator-cores. *Entropic's current STB products are summarised at:* Entropic