

Institution:	University of Warwick
Unit of Assessment:	B9 Physics
Title of case study:	Impact of research into strained silicon on the electronics and energy sectors
<p>1. Summary of the impact</p> <p>Research carried out at Warwick into the growth of silicon-based layered semiconductors has had a variety of impacts in the fields of microelectronics and solar energy generation. In 2004, a spin-out company <i>AdvanceSis</i> was created to exploit the patent portfolio of Warwick's NanoSilicon Group, with an initial £300 k of Regional Development Fund support. The company, having focused on the business of solar energy generation through concentrator photovoltaic (CPV) technology and renamed <i>Circadian Solar</i>, was valued at £3.5 million by the end of 2011. Further impact of the Warwick silicon research, in the period since 2008, has come in the form of joint R&D programmes with companies in the electronics and ICT sectors, including supplying advanced semiconductor materials and by providing highly skilled employees trained in the research group.</p>	
<p>2. Underpinning research</p> <p>Most computers worldwide now contain strained silicon. In essence, strain distorts the Si crystal lattice, allowing electrons within it to travel faster. This improves microprocessor speed and has been employed by Intel since the 90 nm technology node in 2000, through the current 22 nm production node, to all planned future transistors. The crucial required understanding of the effects of strain arose from research on SiGe epitaxy (the controlled deposition of material in sequential atomic layers), in which the Warwick NanoSilicon research group has played a significant part. The group was established in 1986 by Prof. Evan Parker and has published over 200 journal papers related to silicon-based epitaxy since 1993 [e.g. 1-3]. From 1997 to 2003, the Warwick Group led the EPSRC "SiGe for MOS Technologies" programme [8], with leading European industrial partners, that both created a UK community in the research field and was instrumental in establishing germanium as an essential component for developing new technologies.</p> <p>Germanium has a much larger hole mobility than Si, which is attractive for the p-channel in CMOS; Ge also has a smaller bandgap than silicon, which gives it advantages as a light absorber within a solar cell or as photon detector. However, the natural spacing between Ge atoms is 4% larger than for Si which makes growing Ge directly on the ubiquitous Si substrate a challenge; strain relaxation during epitaxial growth can lead to a very high density of dislocations that is detrimental to device performance. So another inventive step was required: during 2000-2004 the Warwick Group embarked on research to create smooth strain-tuning buffers ('virtual substrates' VS that enable a transition from the Si substrate to an arbitrary SiGe alloy, with the surface layer being fully relaxed). The threading defect density was reduced from above 10^{10}cm^{-2} to below 10^6cm^{-2} (an acceptable level for device processing) whilst maintaining a surface roughness below a few nanometres for a $\text{Si}_{0.5}\text{Ge}_{0.5}$ alloy [4] and ~ 1 nm for a 20% Ge alloy. Silicon layers grown on top of these platforms would be biaxially compressive strained, whilst Ge layers would be tensile strained. The novelty of the Warwick approach came in the method of increasing the $\text{Si}_{1-x}\text{Ge}_x$ alloy composition through the virtual substrate (from $x=0$ at the Si substrate) and in the initial surface preparation. This research in novel types of epitaxial growth led to a portfolio of patents [7], which in turn led to the creation of the spin-out company <i>AdvanceSis</i> for their exploitation.</p> <p>In a parallel development by the NanoSilicon group working with <i>AdvanceSis</i>, fully relaxed Ge layers were produced directly on Si through a two-step growth procedure: a thin initial 'seed layer' of Ge is deposited at a low growth temperature, which accommodates the change in lattice parameter by forming a dense network of dislocations; a second thicker layer of Ge is grown at much higher temperature that encourages dislocation glide and annihilation, resulting in a smooth relaxed Ge surface. Such material was shown to be suitable for solar photovoltaic and infrared detector applications [5]. These platforms also provided a route to integrating Ge and III-V semiconductor heterostructures (such as used for LEDs and laser diodes) onto silicon, which opens the possibility of combining the processing power of silicon electronics with the added optical functionality of the other materials.</p> <p>Finally, these two developments were combined to create 'reverse graded virtual substrates' that</p>	

start from a relaxed Ge layer grown by the two-temperature method and then decrease the Ge fraction from $x=1$ in a series of $\text{Si}_{1-x}\text{Ge}_x$ alloy layers [6]. With such structures the substrate required to support a strained Ge layer can be much thinner, and of better quality, than with conventional forward grading. Indeed, we have produced a two-dimensional hole gas with a low-temperature mobility of over $1.5 \times 10^6 \text{cm}^2/\text{Vs}$ in such a strained Ge heterostructure.

A vital factor in enabling impact, was the major investment by Warwick in an industrially compatible epitaxy system (2003). The ASM Epsilon 2000E reduced pressure chemical vapour deposition tool enabled us to produce wafers meeting the exacting standards of industry, in sufficient quantity.

Principal Warwick Researchers: Prof. Evan Parker (1986-2013), Prof. Terry Whall (1987-2013), Prof. David Leadley (1995-2013); Rob Lander (PhD 1993-97, RA 97-98), Tim Grasby (PhD 1996-00, RA 00-03), Maksym Myronov (PhD 1997-2001, SRF 08-13), Martin Palmer (PhD 1997-01), Adam Capewell (PhD 1998-02, RA 02-03), Dominic Fulgoni (PhD 1998-02, RA 02-03), Lee Nash (PhD 2001-05), John Parsons (PhD 2004-07), Andrew Dobbie (PhD 2003-07, RA 07-11), Vishal Shah (PhD 2005-09, RA 09-13), Stephen Thomas (PhD 2006-10).

3. References to the research (Warwick authors in bold)

Publications:

1. **R.J.P Lander**, M.J Kearney, A.I Horrell, **E.H.C Parker**, **P.J Phillips** and **T.E Whall**. "On the low-temperature mobility of holes in gated oxide Si/SiGe heterostructures", *Semicond. Sci. Technol.* **12**, 1064 (1997). Cited 31 times. DOI: [10.1088/0268-1242/12/9/002](https://doi.org/10.1088/0268-1242/12/9/002)
2. **T.E Whall** and **E.H.C Parker**. "SiGe heterostructures for FET applications", *J. Phys. D* **31**, 1397 (1998). Cited 53 times. DOI: [10.1088/0022-3727/31/12/003](https://doi.org/10.1088/0022-3727/31/12/003)
3. **M. Myronov**, T. Irisawa, O.A. Mironov, S. Koh, Y. Shiraki, **T.E. Whall**, and **E.H.C. Parker**. "Extremely high room-temperature two-dimensional hole gas mobility in Ge/Si_{0.33}Ge_{0.67}/Si(001) p-type modulation-doped heterostructures", *Appl. Phys. Lett.* **80**, 3117 (2002). Cited 45 times. DOI: [10.1063/1.1473690](https://doi.org/10.1063/1.1473690)
4. **A.D. Capewell**, **T.J. Grasby**, **T.E. Whall**, and **E.H.C. Parker**. "Terrace grading of SiGe for high-quality virtual substrates", *Appl. Phys. Lett.* **81**, 4775 (2002). Cited 15 times. DOI: [10.1063/1.1529308](https://doi.org/10.1063/1.1529308)
5. L. Colace, G. Assanto, **D. Fulgoni**, and **L. Nash**. "Near-Infrared p-i-n Ge-on-Si Photodiodes for Silicon Integrated Receivers", *J. Lightwave Technol.* **26**, 2954 (2008). Cited 5 times. DOI: [10.1109/JLT.2008.925032](https://doi.org/10.1109/JLT.2008.925032)
6. **V.A. Shah**, **A. Dobbie**, **M. Myronov**, **D.J.F. Fulgoni**, **L.J. Nash**, and **D.R. Leadley**. "Reverse graded relaxed buffers for high Ge content SiGe virtual substrates" *Appl. Phys. Lett.* **93**, 192103 (2008). Cited 24 times. DOI: [10.1063/1.3023068](https://doi.org/10.1063/1.3023068)

Patents:

7. **A.D. Capewell**, **T.J. Grasby**, **E.H.C. Parker** and **T.E. Whall**, "Formation of Lattice-Tuning Semiconductor Substrates", [PCT WO/2003/103031](https://patents.google.com/patent/PCT/WO/2003/103031) (2002), [PCT WO/2004/023536](https://patents.google.com/patent/PCT/WO/2004/023536) (2002), [PCT WO/2005/048330](https://patents.google.com/patent/PCT/WO/2005/048330) (2003), [PCT WO/2006/032681](https://patents.google.com/patent/PCT/WO/2006/032681) (2004).

Grants:

8. EPSRC: *SiGe for MOS Technologies*, (1997-2004). £7.3 M of linked grants at Cambridge, Glasgow, Imperial, Loughborough, Manchester, Newcastle, Sheffield, Southampton and led by Warwick ([GR/L53793/01](https://doi.org/10.1033/978113593793001), [GR/N65691/01](https://doi.org/10.1033/978113593791001)), incorporating Avant!, Daimler-Chrysler, Infineon, Mitel Semiconductors (Zarlink), QinetiQ, and Siemens. *New Generation SS-MBE Growth System for Silicon Heterostructures* ([GR/R62519/01](https://doi.org/10.1033/9781135937251001)) 2002-2005 £200k; *Renaissance Ge*, ([EP/F031408/1](https://doi.org/10.1033/978113593714081)) 2008-2012, £1 M
9. EU FP6 Network of Excellence *Silicon-based nanodevices (SINANO)*, 2004-07, €10 M with 48 European institutes; FP7 NoE *Silicon-based nanostructure and nanodevices for long-term nanoelectronics applications (NANOSIL)* 2008-11, €4.3 M with 28 partners; FP7 NoE *NANOFUNCTION* 2010-13, €3 M with 16 partners. FP6 Integrated Project *Pulling the limits of nanoCMOS electronics (PULLNANO)*, 2006-08, €45 M project with 36 partners, led by STMicroelectronics.

4. Details of the impact

The research described above, and in particular development of virtual substrates and Ge epitaxy, led to the launch of a spin-out company in 2003. Starting with £2 M of venture capital funding and six employees, *AdvanceSis* aimed to commercialise outputs from Warwick's NanoSilicon Group patent portfolio [7]. *AdvanceSis* was initially nurtured within the Dept of Physics, with a minimum of bureaucracy and full access to facilities. This enabled the company rapidly to develop both the epitaxial know-how and business acumen required for expansion [10]. In 2005, *AdvanceSis* won the Lord Stafford Award for 'Best University Spin Out'. A significant aspect of the business was to supply Ge-on-Si wafers into the R&D programme of a major semiconductor company that led (in 2009) to a prototype short-range optical link using Ge detectors. *AdvanceSis* were complimented on producing much higher quality wafers than other sub-contractors and delivering to schedule.

AdvanceSis moved to its own premises on the University of Warwick Science Park in 2008 and identified a market niche in solar-power generation by concentrator photo-voltaic (CPV) technology, initially using Ge solar cells. To reflect this, in 2009 the company changed its name to *Circadian Solar* [11]. By improving the efficiency of both the solar cell material, advanced optics and sun-tracking control systems accurate to 0.4°, *Circadian Solar* made 30 m² systems of CPV modules that were more than twice as efficient as typical commercial Si panels and could produce solar electricity at close to the critical \$1/W fully installed cost in regions with high levels of sunshine [12]. As chairman of the board, Prof. Parker assisted the company, between 2003 and 2010, in raising a further £12 M from Seven Spires Investments Ltd., who saw

“excellent management, defensible Intellectual Property, a well characterised route to market and global scalability to an expected market capitalisation in excess of \$100 M.” [13]

In 2010, *Circadian Solar* was ranked 16th on a list of top university spin-out companies [14] and, by the end of 2011, was established as a fully independent company employing 35 people and with a 'net worth' of £3.5 M [15].

Employees include a number of researchers trained to PhD level in the NanoSilicon Group (Parsons, Nash, Fulgoni, Palmer, Capewell) and also ex-motor industry workers from the West Midlands. Coventry South MP spoke of the importance of the company whilst visiting in 2009:

“The Midlands used to be the home of the automotive industry so this region has been one of the hardest hit by job losses resulting from the recession. Now we need to look to new industries such as solar power to revitalise the region and help move us towards a low carbon economy. We have the facilities, design expertise and skilled workforce in place to capitalise on any investment made into this fledgling industry that has such great potential.” [16]

The growth of the company has generated business and employment for sub-contractors not only in the UK but also abroad. In 2009, *tf2 devices B.V.* was created as a joint venture with Radboud University, Nijmegen, [17] to exploit the epitaxial lift-off process for III-V semiconductors used to make *Circadian's* CPV modules. As part of the company's plan to demonstrate cost-effective energy yield in different regions and environments module evaluation was performed in Cyprus in late 2008, and in 2010 *Circadian* established a test facility for its CPV solar energy system in Lisbon to take advantage of the high level of direct sunlight in Portugal [12].

With the solar cell market in 2013 being dominated by Chinese state subsidised large-area, low-efficiency silicon panels (having a fully installed cost of well under \$1/W), many solar companies across the Western world have collapsed. By contrast, *Circadian Solar* survived (albeit with a reduced valuation in July 2013 of £1.5 M). The major impact in the REF Impact period has thus been to directly generate employment and through the spending of over £10 M in the economy including sourcing components from sub-contractors.

Impact has also been achieved through:

(i) **Collaborating with Industry on Research** – Many European companies started work in the SiGe field during the 1990's; the Warwick group collaborated and published with Daimler-Chrysler, Philips, Siemens (Infineon, Quimoda), ST Microelectronics among others. In the REF period, we have supplied several industrial collaborators with extremely high quality epitaxial material. For example, in 2008-10, Warwick supplied 120 epitaxial wafers of Ge layers on Si substrates to IMEC, where the transistors were fabricated in a silicon industry compatible 65 nm process by Intel employees to create the first strained-Ge transistors [18]. In 2009, over 100 wafers were supplied

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to MPI Halle for developing a layer transfer process to create Ge-on-insulator platforms. We have also applied our expertise and characterisation facilities to analyse devices made by companies. In a joint activity with device modellers from University of Udine, NXP Semiconductors (now part of TSMC) benefitted from a greater understanding of their FinFET devices [19]:

“Key to building this understanding is the development and experimental verification of charge transport models. The characterisation ... performed by the Warwick team has led to new insights and supported greatly the development of predictive transport models that can be incorporated into device simulation tools. In this way the expertise and capabilities of the Warwick team have impacted both the development costs and development time of novel finFET-based CMOS technologies.” [20]

TSMC is now entering production with 20 nm node FinFETs [21], and these could well become 20% of their \$14 B annual revenue within the next 10 years.

(ii) **Industrially Relevant Training** – PhD students and PDRAs in the Group have not only developed expertise in using advanced equipment for fabrication and characterisation of semiconductor devices, but have also engaged with our collaborative partners (mentioned in (i) above). This has included making use of exchange programmes with companies through the SiNANO networks [9, 22] that Parker and Leadley played a pivotal role in setting up. 15 PhD graduates and PDRAs from the NanoSilicon Group (list available on request) have gone on to use their specific expertise working for a number of companies and research institutes incl. AmberWave, IMEC, International Rectifier, IQE, NXP, Philips, QinetiQ, Sharp, VG Semicon, and Circadian Solar. These employed researchers have continued to contribute to high technology development and to the economy throughout the REF Impact period.

5. Sources to corroborate the impact (Warwick authors in bold, industrial authors in red)

10. Letter received from CEO of Circadian Solar
11. Company website: www.circadiansolar.com
12. Review article from Renewable Energy World (Dec. 2010). tinyurl.com/qc4s9c9
13. Seven Spires Investments Ltd. sevenspires.co.uk
14. Circadian Solar ranked 16th (The Daily Telegraph, 2010). tinyurl.com/qcmzxk2
15. Financial Accounts as filed 10/04/2013 at Companies House
16. Coventry South MP speaking while visiting Circadian Solar in 2009 and reported in various media such as Solar Magazine. tinyurl.com/oh8wllak
17. Company website: tf2devices.com
18. With **IMEC** and **Intel** and presented as a talk at the major Asian microelectronics conference SSDM (2010): **J Mitard, B De Jaeger, G Eneman, A Dobbie, M Myronov, M Kobayashi, J Geypen, H Bender, B Vincent, R Krom, J Franco, G Winderickx, E Vrancken, W Vanherle, W Wang, J Tseng, R Loo, K De Meyer, M Caymax, L Pantisano, D.R. Leadley, M Meuris, P. Absil, S Biesemans, and T Hoffmann** “High hole mobility in 65nm strained Ge-pFETs with HfO₂ gate dielectric” Jap. J. Appl. Phys. **50**, 04DC17 (2011) DOI: [10.1143/JJAP.50.04DC17](https://doi.org/10.1143/JJAP.50.04DC17)
19. With **IMEC** and **NXP-TSMC**: F. Conzatti, N. Serra, D. Esseni, M. De Michielis, P. Palestri, L. Selmi, **S.M. Thomas, T.E. Whall, D.R. Leadley, E.H.C. Parker, L. Witters**, M.J. Hütch, E. Snoeck, **T.J. Wang, W.C. Lee, G. Doornbos, G. Vellianitis, M.J.H. van Dal, and R.J.P. Lander**, Investigation of strain engineering in FinFETs comprising experimental analysis and numerical simulations, IEEE Trans. Electron Dev. **58**, 1583-1593 (2011) DOI: [10.1109/TED.2011.2119320](https://doi.org/10.1109/TED.2011.2119320)
20. Email from Senior Principal Scientist at NXP Semiconductors (now at Sharp Europe).
21. “TSMC Shows Path to 16nm, Beyond” *EE Times* (2013) www.eetimes.com/document.asp?doc_id=1319679
22. SiNANO Institute, created as legal entity under French law in 2008. Website: www.sinano.eu