Institution: Newcastle University

Unit of Assessment: 13: Electrical and Electronic Engineering

Title of case study: Worldwide Industrial Adoption of Asynchronous System Design

1. Summary of the impact

Newcastle University's fundamental research into the automated synthesis of asynchronous systems and metastability analysis has resulted in new technologies that have been adopted worldwide by the microprocessor industry and educational sectors. In particular, Newcastle's asynchronous design methods and tools based on Petri nets have been used by the industry leading vendor Intel Corporation for their switch silicon technology, on which most transactions on the NYSE and NASDAQ (with combined daily volume of trade exceeding £80 billion) now rely. Oracle Corporation used the results of Newcastle's metastability analysis research for building their SPARC series of servers, marketed as having "world's fastest microprocessor".

2. Underpinning research

The main research findings underpinning the presented impact are based on the longstanding investigations in the two connected domains of asynchronous systems design, namely:

(a) developing methods for modelling, analysis and synthesis of asynchronous (self-timed) circuits, led by Alex Yakovlev *(Lecturer/Reader/Professor of Computer Systems Design: 1991 - present);*

(b) providing better understanding and characterisation of metastability in electronic systems and design of robust arbiters and synchronisers, led by Prof. David Kinniment (*Professor since 1979, Newcastle University*).

A strong link between the domains (a) and (b) exists in many current industrial developments that use networks on chip, multi and many-core processors, and systems with severe power constraints. The design of communication fabrics in complex systems on chip becomes increasingly more asynchronous (domain a). This creates a large demand for design techniques to interface these communication fabrics to local data processing cores, and such interfaces need to provide high performance reliable synchronization to the local timing regions (domain b).

In (a), research has provided a solution to the longstanding problem of developing a modelling technique that describes concurrent behaviour of asynchronous systems. The foundations of our contributions in this area were established since the 1990s when Prof. Yakovlev produced the unified model of *Signal* Transition *Graphs* (STG) [P1], which has now become a *standard notation* for synthesis of controllers and interfaces in multi-synchronous systems on chip. This model and associated tools have a pivotal role in making Petri nets a formal semantic kernel of the new asynchronous system design flow, similar to that of finite state machines in synchronous system design. The STG model has given a way to capturing highly concurrent behaviour typical for asynchronous systems in a very compact form, without exponential state explosion inherent in state machine modelling methods.

Newcastle's joint research on synthesis methods using STG & Petri nets with collaborators from Polytechnics of Catalonia and Turin, Cadence and Intel Corporation has produced the software tool *Petrify.* This tool, described in a widely cited paper [P2], was released into the public domain in 2000 and subsequently has become widely used in academia and industry. The key innovative features of the new synthesis method used in Petrify was the development and application of *theory of regions* to *solving complete state coding* in STGs, implementation of STG specifications in *semi-modular and speed-independent circuits*, and the development and application of the idea of *relative timing* for logic optimisation. They are all described in the monograph [P3] that, together with the Petrify tool, was awarded the status of Finalist in the 2002 Descartes Prize competition.

In (b), research has focussed on the problem of *accurate characterisation of metastability,* developing practical methods for *on-chip* measurement of *deep metastability,* evaluating the effects of *front and back edges of the clock on metastability resolution time,* characterising *failures*

and mean-time between failures (MTBF) in a range of synchronisers [P4].

Over the last decade, the industrial need for accurate modelling of metastability and for robust synchronisers has steadily increased, due to the rapid growth of computer system complexity. Newcastle's *robust synchronisers*, based on *supply voltage adaptation and pipelining*, are crucial to the reliability of modern and future computer systems because they consist of hundreds of processors, independently clocked, powered and connected by asynchronous networks. This research has lead to identifying an important *design trade-off between synchronization time and reliability*. In the EPSRC-funded project (SYRINGE), in collaboration with Intel Corporation, Newcastle's researchers developed innovative methods of metastability analysis and design of robust synchronisers which have extended mean-time between failures (MTBFs) to 3-5 years [P4].

In 2008, the proposed on-chip metastability measurement techniques were applied to develop a new robust synchroniser *tolerant to variations in voltage supply, external temperature and process variability* [P5]. This work was later extended, in collaboration with IMEC Netherlands, to the characterisation of the performance of synchronizers in the sub-threshold mode [P6], thereby enabling ultra-low power applications in medicine and energy-harvesting.

3. References to the research

[P1] A. Yakovlev, L. Lavagno and A. Sangiovanni-Vincentelli. "*A unified signal transition graph model for asynchronous control circuit synthesis*". Formal Methods in System Design (Kluwer), Vol. 9, No. 3, Nov. 1996, pp. 139-188.

[P2] J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, and A. Yakovlev: "*Petrify: a tool for manipulating concurrent specifications and synthesis of asynchronous controllers"*. IEICE Trans on Inf. and Syst. E80-D(3): 315-325 (1997). Google Scholar: 500+ citations. [*key ref.]

[P3] J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno and A. Yakovlev. *Logic Synthesis of Asynchronous Controllers and Interfaces*, Springer Series in Advanced Microelectronics, vol. 8, Springer, 2002, ISBN-3-540-43152-7. [*key ref.]

[P4] D.J. Kinniment, Ch. E. Dike, K. Heron, G. Russell and A. Yakovlev. "*Measuring Deep Metastability and Its Effect on Synchronizer Performance*". IEEE TVLSI 2007, 15(9), 1028-1039.

[P5] D.J. Kinniment. *Synchronization and Arbitration in Digital Systems,* UK: Wiley and Sons, 2007 (with contributions from A.Bystrov, M. Renaudin, G. Russell and A. Yakovlev) [*key ref.]

[P6] J. Zhou, M. Ashouei, D. Kinniment, J. Huisken, G. Russell and A. Yakovlev. "*Sub-threshold Synchronizer*", Microelectronics Journal, vol.42, no.6, June 2011, pp. 840-850.

Key Research Grants (*final reports are available on http://async.org.uk*)

EP/E044662/1, £371,922, 01/07/07-30/06/10, Self-Timed Event Processor (STEP), PI: A. Yakovlev. Collaboration with MBDA UK Ltd.

EP/C007298/1, £219,200, 1/07/05-30/06/05, Synchronizer Reliability in the Next Generation of SoC with Multiple Clocks (SYRINGE) , PI: A. Yakovlev. Collaboration with Intel Corp.

GR/S12036, £244,563, 1/01/03-31/12/05, Synthesis and Testing of Low-Latency Asynchronous Circuits (STELLA), PI: A. Yakovlev

GR/R16754, £325,000, 1/07/2001-31/09/2004, (IRG evaluation – internationally leading, outstanding), Behavioural Synthesis of Systems with Heterogeneous Timing (BESST), PI: A. Yakovlev.

GR/R32666 and GR/R32895 (via Kingston Univ.), £340,000, 1/07/2001-17/11/2004, Computational Heterogeneously Timed Networks (COHERENT), PI: A. Yakovlev, Collaboration with MBDA UK.

GR/L93775, £162,000, 1/05/97-31/10/2001, (IRG evaluation – internationally leading, outstanding), Asynchronous communication mechanisms for real-time systems (COMFORT), PI: A. Yakovlev, Collaboration with MBDA UK Ltd.

GR/K70175, £120,000, 1/10/96-29/02/2000, (evaluation: alpha 5, excellent), Hazard-free arbiter design (HADES), PI: A. Yakovlev

GR/J52327, £115,000, 1/12/93 - 1/6/97 (evaluation - alpha 5, excellent), Automated synthesis of parallel synchronous and asynchronous controllers (ASAP), PI : D.J. Kinniment

4. Details of the impact

In the current environment where there is increasing demand for volume and speed of electronic activity combined with environmental concerns, asynchronous chips (a faster and more power efficient technology) has been welcomed by industry and users. The pathway to this impact has been, over the last 20 years, laid through influential research dissemination by the Newcastle group, having the highest publication track record in the history of the IEEE International Symposium on Asynchronous Circuits and Systems, amongst the entire international asynchronous circuits and systems community. Newcastle has had close and never-stopping interaction with the industrial members of this community, which includes several leading scientists and engineers from Intel, Sun (now Oracle), Fulcrum (now Intel).

The research has enabled automated construction of asynchronous circuits

The results of research described in this case study have been used as the basis for Intel Corporation's Computer Aided Design (CAD) tools for asynchronous circuits. In his letter [E3], Intel's Chief Scientist for Technology Development identified the longstanding problem of high levels of complexity that the inherent concurrency of asynchronous circuits pose to industrial designers, and stated that "*The predominant means of analysing this concurrency is Petri Nets and the work by Alex Yakovlev and his colleagues have pioneered the application of Petri Nets to asynchronous circuits"* [E3].

Specifically STGs, Petrify and related Petri net theories have provided (i) the basis of understanding and modelling performance analysis as well as optimisation of asynchronous circuits, and (ii) the formal basis of the *slack matching* optimisation algorithm (patented by Fulcrum Microsystem [E4]) which is a key technology for asynchronous circuits design. In combination, together, (i) and (ii) have allowed Intel to produce higher performance asynchronous circuits ("*Slack matching is one of the core technologies within the asynchronous CAD flow that my Intel division is using and this process is a pillar to us achieving higher performance than the synchronous alternatives in our past two products*" [E3]).

Intel's press release on the acquisition of Fulcrum Microsystems stated: *"Fulcrum Microsystems' [asynchronous] switch silicon, already recognized for high performance and low latency, complements Intel's leading processors and Ethernet controllers, and will deliver our customers new levels of performance and energy efficiency while improving their economics of cloud service delivery."* [E8].

The impact is evident in the wide deployment of the new circuits in the financial services industry; in particular, most transactions on the NYSE and NASDAQ (combined daily volume of trade exceeding £80 billion) now rely on Intel's switch silicon – a design facilitated by the use of new CAD tools that depend on the research described earlier [E3]. Gartner Analysts reported that for the years 2010-2012 the total annual worldwide semiconductor revenue was on average $300 billion. Intel Corporation had 16% of this market and was the world leading manufacturer of chips for high-performance computers ("*no.1 semiconductor vendor for the 21st year in a row*").

Tools & techniques for improving synchroniser design has been adopted by industry

Intel Corporation and Sun Microsystems (now Oracle Corporation) have used research results to improve measurement techniques and robustness in their synchronisers. Benefits include new circuits and the valuable analysis capability of new tools, the ideas for which were triggered by Prof. Kinniment's methods to measure deep metastability and MTBF (*Mean Time Between Failures*). The research has allowed better understanding of metastability, improved confidence in performance estimation of circuits and enabled previously unknown effects to be revealed, which significantly enhances system reliability [E1, E2].

As a result, faster and more power efficient synchronisers have been produced by Sun Microsystems in their desktop and server machines (Sun UltraSparc series), during 2008-2009

(and pre-2008). From 2010 Oracle (who bought Sun Microsystems) has continued using research results to create the improved SPARC series of products [E2]. As a result of using synchronisers that have been designed and characterised using Newcastle's methods Oracle have been able to scale up the performance of their processors without reducing their reliability. The SPARC processors are world leaders in terms of processing speed and several records have been broken [E5, E6] allowing Oracle to compete with other providers like IBM. The Transaction Processing Performance Council, whose membership includes the major businesses in the field, indicate Oracle SPARC products as top ranking in the performance category [E7].

In 2013, the SPARC microprocessor was released by Oracle as the world's fastest microprocessor [E6]. Quote from John Fowler, executive vice president, Systems, Oracle: "*The new SPARC T5 and M5 systems leapfrog the competition with up to 10x the performance of the previous generation, offering an unbeatable value for midrange and high-end enterprise computing*" [E6].

Other notable impacts

Other beneficiaries include Spanish company *Elastic Clocks*, who in collaboration with Newcastle during 2008-2010 gained improvements in their industrial EDA flow and achieved on average up to 30% power savings in microprocessor chips while maintaining performance. More recently, the company *Dialog Semiconductor* with offices in USA, Europe and East Asia released a series of power efficient products (www.dialog-semiconductor.com/) designed using the tools provided by the research.

Due to the uptake by industry the research described in Section 2 is now an embedded element of teaching practice in asynchronous design, demonstrating that this vital area of *professional training* has been informed and stimulated by research at Newcastle University. The impact on Higher Education extends significantly beyond Newcastle University and now around the world, most of the top engineering courses use *Petrify* and STGs in courses on asynchronous circuit design (e.g. Columbia University in the USA, Technical University of Vienna in Austria, and IIT Delhi in India). [E9] shows an example of course material used. As Intel's Chief Scientist for Technology Development [E3] testifies: *"The tool Petrify and STGs have become a fantastic means of teaching and explaining asynchronous design concepts".*

5. Sources to corroborate the impact

[E1] Corroboration from Intel Strategic CAD Labs

[E2] Corroboration from Oracle Labs

[E3] Corroboration from Intel Corporation.

[E4] Patent by Fulcrum Microsystems & University of Southern California (US 8495543 B2, US 20110029941 A1, WO 2009155370 A1). http://www.faqs.org/patents/app/20110029941

[E5] Press release "*Oracle's SPARC T3 Servers Deliver World-Record Performance Results*" http://www.oracle.com/us/corporate/press/173541. (2010) Oracle OpenWorld.

[E6] Press release "*Oracle Unveils SPARC Servers with the World's Fastest Microprocessor",* http://www.oracle.com/us/corporate/press/1923343, (2013) Oracle, Redwood Shores.

[E7] TPC-C - Top Ten Performance Results, http://www.tpc.org/tpcc/results/tpcc_perf_results.asp. Transaction Processing Performance Council (2013)

[E8] Press release on acquisition of Fulcrum by Intel: http://newsroom.intel.com/community/intel_newsroom/blog/2011/07/19/intel-to-acquire-fulcrum-microsystems (2011)

[E9] Teaching material of TU Vienna: http://ti.tuwien.ac.at/ecs/teaching/courses/adide_WS_2012/add-exercise-assignments-1/add-design-assignment-3 (Dec. 2012)