

Institution: University of Essex
Unit of Assessment: 11 – Computer Science and Informatics
Title of case study: UltraSoC: Commercialisation of a novel debug support architecture for multi-processor systems on a chip
<p>1. Summary of the impact</p> <p>From 2005, a body of research undertaken at the University of Essex has developed a novel debug support architecture for systems on a chip (SoC). This platform successfully addresses the challenge of debugging applications executing on SoCs with multiple processor cores. A system-centric architecture is used, which achieves substantial improvement in compression and requires dramatically less silicon real estate than existing state of the art applications. The research underpins 'UltraDebug', which is commercialised via the spin-out 'UltraSoC'. UltraSoC has attracted investment worth £5million (the majority coming from venture capital sources) and is currently working with PMC-Sierra to incorporate its innovative technology into PMC's next generation of storage controllers.</p>
<p>2. Underpinning research</p> <p>System on a chip (SoC) technology has become ubiquitous and multiprocessor systems on a chip (MPSoC) are increasingly used in embedded systems. Such platforms are becoming commonplace in everyday life and underpin a vast array of consumer items including cars, mobile phones and household goods. The successful development of these products relies on chip debugging in a short timeframe. However, the advancement of SoC technology, and particularly the move towards MPSoCs, has rendered previous application software debugging strategies obsolete, unreliable or insufficient. Traditionally these strategies have been focussed on providing debug support for chips comprising single processors, or multiple processors of a specific family of processor architectures. They have not kept pace with the widening diversity of processor cores employed on SoCs.</p> <p>Beginning in 2001, research led by Professor Klaus McDonald-Maier whilst he was at the University of Kent identified the need for support of software application development in SoC architectures, particularly in cases where complex software is required to interact and execute on multiple processor cores. In cases where SoCs feature other highly interactive blocks (which may contribute to undesired behaviour of the system), this presented a significant technical challenge. In 2005 McDonald-Maier and his team moved to Essex. Between 2005 and 2008 he worked with Andrew Hopkins (who joined Essex as a Senior Researcher in 2005, and from April 2010 to February 2011 held the role of Visiting Research Fellow) on an EPSRC funded project that developed these initial concepts into practical implementations. Their research produced a highly modular debug support architecture, consisting of two important stages. Firstly, debug support adapters were provided in order to connect each processor core, peripheral or interconnect, to the debug infrastructure. The second stage then controlled these adapters, combining their debug data streams in order to preserve timing and compress resulting data to an absolute minimum. Critically, this compression meant that debug data could be straightforwardly sent from the SoC to an external development station or PC using a limited bandwidth interface. This would be an important characteristic given the high volume of devices requiring this infrastructure to be added.</p> <p>The development of this process represented the first systems-centric debug support architecture for SoCs featuring multiple hybrid processor cores (as well as other active peripherals). The architecture substantially outperformed the state of the art and, notably, achieved this in a</p>

Impact case study (REF3b)

significantly more compact implementation than existing architectures. The developed process could offer debug support for two processor cores using less logic than that required for one processor core when using previous state of the art.

3. References to the research

Hopkins, A.B.T. and K.D. McDonald-Maier (2006) Debug Support Strategy for Systems-on-Chips with Multiple Processor Cores, *IEEE Transactions on Computers*, 55(2), 174-184. (66 citations – November 2013) DOI:10.1109/TC.2006.22

Hopkins, A.B.T. and K.D. McDonald-Maier (2006) Debug support for complex Systems on-Chip: A review, *IEE Proceedings on Computers and Digital Techniques*, 153(4), 197-207. (91 citations – November 2013) DOI:10.1049/ip-cdt:20050194

Mayer, A., H. Siebert and K.D. McDonald-Maier (2007) Boosting Debug Support for Complex Systems-on-Chip, *IEEE Computer*, 40(4), 76-81. (26 citations – November 2013) DOI:10.1109/MC.2007.118

Research funding:

McDonald-Maier, *Debug support strategy for systems-on-chips with multiple processor cores*, (EPSRC Research Grant GR/S13361/02), Aug '05 – May '06, £39,218 (This grant was transferred from the University of Kent, where it had the reference GR/S13361/01)

McDonald-Maier, *ReSIP – Reconfigurable system-on-chip based networks of integrated and distributed sensor platform nodes for environmental diagnostic and sensing*, (EPSRC Research Grant EP/C005686/1), Oct '05 – Sep '08, £265,844

McDonald-Maier, *Networking of distributed sensors for proactive condition monitoring of wind*, (EPSRC Research Grant EP/C014790/1), Oct '05 – Jan '09, £213,374

McDonald-Maier, *ESPACENET – Evolvable networks of intelligent and secure integrated and distributed reconfigurable system-on-chip sensor nodes for aerospace based monitoring and diagnostics*, (EPSRC Research Grant EP/C54630X/1), Oct '05 – Nov '08, £268,856

4. Details of the impact

The research group at Essex recognised that the outputs of their work held broad applicability for providing debug support to MPSoCs in a vast array of global scenarios that rely on embedded systems. In a marketplace where nearly half the cost of chip development is currently spent on debugging activities, the novel architecture resulting from the research conducted at Essex could be used to write much more reliable software. This would have significant economic and safety implications in consumer electronics and safety-critical applications. Essex researchers sought to share the capabilities and associated benefits of this technology with a wide audience, and developed a robust strategy in order to transform research insight into practical benefit. This centred on a broad range of dissemination activities that targeted investment from a variety of sources, in order to help commercialise the technology. Initial activities, undertaken by the group in translating research towards impact between 2005 and 2008, have been well documented in external media. In providing detail, this account initially draws on corroborating sources produced by: [1] Praxis Unico; [2] The Industrial Systems Institute, Patras, Greece and; [3] RCUK.

In 2005, the group founded 'UltraSoC' to commercialise the practical implementations to be developed from research [see corroborating source 1]. The group began to actively seek funding that could be used to develop their initial concept, with the aim of marketing and delivering a commercial product. In 2006, an initial proof of concept was produced, aimed at the automotive market and supported by the South East Seed Fund [2]. In the same year UltraSoC was also a finalist in the RCUK business plan competition and received £10k to further develop the business plan [3]. The group continued to enter competitions and apply to programmes which could support further development of their growing market potential. In 2007 UltraSoC was shortlisted for the *Software in Design* award, as part of the IET *Innovation in Engineering* awards. The group also reached the final stages of the East of England Development Agency's *Running the Gauntlet* competition [2].

In 2008, UltraSoC became a joint spin-out from the Universities of Essex and Kent [2]. The group's proactive approach to seeking funding and investment had not only attracted financial support, but critically it had also generated significant market exposure for their technology. In 2009 UltraSoC received seedcorn funding worth £400k from the South East Seed Fund and the IcenI seedcorn fund [1]. This allowed the company to open a Cambridge office and produce a commercial demonstrator of their technology, named 'UltraDebug'. This represented the first commercial implementation of the group's research and offered a highly flexible platform to provide application-level debug support to multiprocessor SoCs [1]. The architecture was designed to enable the embedded systems industry to create more advanced and reliable products in a range of domains, such as the automotive and consumer device markets. Embodying the novel features of the group's research, UltraDebug provides source-level debugging with superior trace and trigger facilities, and represents a step change in performance compared to existing commercial offerings. In 2010, UltraSoC received a Series A investment of £2million from venture capitalists Octopus Ventures [4]. This enabled development of the UltraDebug platform into a licensable product. Following excellent progress both in technical and commercial programmes Octopus continued to support UltraSoC, awarding a Series A+ investment of £1million in October 2012, followed by a further £1.5million in 2013. The company is now funded to a total of approximately £5million, of which venture capital forms the majority. The remainder is provided by public sources including RDAs and the TSB [5].

In May 2013, UltraSoC announced that it was working with its first customer, the American semiconductor company PMC-Sierra, which develops and sells devices in the communications, storage, printing and embedded-computing markets. The development programme, which is expected to lead to PMC taking a license to the IP, incorporates UltraSoC's innovative technology into PMC's next generation of storage controllers. It places UltraDebug at the leading edge of PMC's embedded systems, and it is anticipated that the technology will be rolled out in chips in the latter part of 2013. The VP of Product Development for PMC's Enterprise Storage Division has acknowledged the significance of partnership with UltraSoC [6], explaining:

"Analyzing complex hardware and software interactions in high-end SoCs requires insight into what is happening through the entire device...PMC partnered with UltraSoC because we recognized that their unique monitoring and debug infrastructure would give us the needed visibility to both enhance our device operation and accelerate our time to market for our customers".

VP Product Development, Enterprise Storage Division, PMC-Sierra

In addition to this large-scale commercial interaction, UltraSoC also remains active in engaging with government-funded development programmes in the UK. In February 2013, the company announced the successful completion of the Debug Platform Development for Automotive Systems (DPD-ASOC) project. The £375k project, part-funded by the TSB and the European Regional Development Fund (ERDF) delivered a debugging demonstrator called 'UltraAuto', which will form the basis of a computational control system to enable reduction of engine carbon emissions, thereby adhering to future EU legislation [7]. UltraSoC has also received further funding under the TSB's Emerging Technologies – Energy Efficient Computing competition. In partnership with the University of Cambridge, this supports the spEEDO (Energy Efficiency through Debug support) project, which began in March 2013 [8].

5. Sources to corroborate the impact [All sources saved on file with HEI, available on request]

[1] Praxis Unico, 2009. *UltraSoC secures seed funding for debugging technology* [online] Available at: <http://www.praxisunico.org.uk/news/member-detail.asp?ItemID=235> [Accessed 23rd July 2013]

[2] I3E, 2011. *UltraSoC: Best Practice Report* [pdf] Patras, Greece, Industrial Systems Institute. Available at: <http://www.i3e.eu/innovation/bestpractices/I3E%20-%20BP%20-%20UltraSOC.pdf> [Accessed 23rd July 2013]

[3] RCUK, 2006. *Winner announced of the 2005/06 Research Council's Business Plan Competition* [online] Available at: <http://www.rcuk.ac.uk/media/news/2006news/Pages/20061208bpc.aspx> [Accessed 23rd July 2013]

[4] Octopus Investments Ltd, 2010. *Octopus partners system-on-chip debug firm UltraSoC Technologies* [online] Available at: <http://www.octopusinvestments.com/news.html?ClickThrough=4&newsId=267> [Accessed 23rd July 2013]

[5] Octopus Investments Ltd, 2013. *Octopus provides further funding to UltraSoC* [online] Available at: <http://www.octopusinvestments.com/news.html?newsId=468> [Accessed 23rd July 2013]

[6] EE Times Europe Analog, 2013. *First universal multicore debug IP delivered to PMC-Sierra* [online] Available at: http://www.analog-eetimes.com/en/first-universal-multicore-debug-ip-delivered-to-pmc-sierra.html?cmp_id=7&news_id=222905083 [Accessed 2nd October 2013]

[7] UltraSoC, 2013. *UltraSoC Successfully Completes Low Carbon Initiators TSB/ERDF Project* [online] Available at: <http://www.ultrasoc.com/?p=965> [Accessed 23rd July 2013]

[8] UltraSoC, 2013. *UltraSoC and Cambridge University awarded Energy Efficient Computing Funding from TSB* [online] Available at: <http://www.ultrasoc.com/?p=1002> [Accessed 23rd July 2013]