Institution: University College London (UCL)

Unit of Assessment: 9 – Physics

Title of case study: Enabling SEMATECH and industrial member companies to improve their transistor technology

1. Summary of the impact

Researchers within the Department of Physics and Astronomy at UCL have investigated the properties of defects in bulk HfO_2 and at $Si/SiO_x/HfO_2$ interfaces. Results have been used by an industrial partner, SEMATECH (SMT), to improve the quality and reliability of high-performance microelectronic devices based on transistors. This has helped SMT to meet project objectives on behalf of member companies such as Intel and IBM, and UCL research results have been consistently highly evaluated by these companies. Recommendations made by SMT have been implemented by industrial partners in their currently manufactured devices, such as the 22nm process technology released by Intel in 2011.

2. Underpinning research

Since 2001, researchers in the Department of Physics and Astronomy at UCL have been investigating how to improve reliability and minimise energy loss in transistors for the microelectronics industry.

Transistors are the fundamental building blocks for all computer chips. Over the last 15 years, the microelectronics industry has used silicon dioxide (SiO_2) to produce seven logic-process generations of transistors, and transistor size has decreased with each generation. However, as transistors shrink, leakage current increases, limiting computer processor performance and increasing energy consumption. Managing that leakage current is crucial for reliable high-speed operation, and is becoming an increasingly important factor in chip design and the reduction of power consumption. The semiconductor industry is also struggling with the heat of chips, which increases exponentially as the number of transistors on a chip increases. Controlling leakage current by using new high dielectric constant (high-k) materials instead of SiO_2 is one of many steps towards making sure that scaling of devices continues and ever smaller transistors run reliably.

High-k dielectrics, such as hafnium dioxide (HfO_2) and hafnium silicates, have been in the spotlight of both scientists and engineers over the last ten years as substitutes for SiO_2 as the gate dielectric in metal-oxide semiconductor field-effect transistors (MOSFETs). However, defects and electron trapping in the dielectric layer of these devices lead to the degradation of their performance and reliability, hampering implementation of these dielectrics in a manufacturing environment.

UCL research in this area focused on modelling defects and their properties in bulk HfO_2 and at $Si/SiO_x/HfO_2$ interfaces. The research during 2001-2007 involved using a wide range of computational methods for modelling defects in insulators [1-3]. The research carried out in 2008-2011 was concerned with the interaction of these defects with grain boundaries in polycrystalline HfO_2 and their effects on the leakage current and breakdown of devices [4, 5]. The embedded cluster method developed at UCL allowed modelling of the electronic structure and spectroscopic properties of defects in high-k oxides with the high accuracy required for predicting their properties. UCL researchers were able to identify specific defects in polycrystalline oxide films and at interfaces by comparing their predicted optical, electron trapping and EPR (electron paramagnetic resonance) spectroscopy properties, and the predicted positions of their electronic energy levels, with experimental data.

Findings of the research included the determination that oxygen vacancies in these oxides can capture up to five electrons. It was also found that these defects can be effectively passivated by H_2N groups, suggesting that an application of an ammonia post-deposition anneal would be more effective than the conventional N_2 ambient [2]. This helped to resolve the concern that extremely

high defect density in this material made it unsuitable for high-volume production. In addition, the size of the electron traps (the electron localisation area) was found to be in the order of 1nm (the electron was found to be spread over three nearby Hf atoms) [1, 3]. UCL researchers also determined characteristics of the oxygen vacancies at the grain boundaries in monoclinic HfO_2 and their diffusion paths [4, 5].

Key UCL researchers: A. Shluger (Principal Research Fellow 1999-2002; Reader 2002-2004; Professor 2004-present), A. M. Stoneham (Professor 1995-2006; Emeritus Professor 2006-2011), J. L. Gavartin (Research Fellow 1998-2005; Senior Research Fellow 2005-2007), D. Muñoz-Ramo (Research Associate 2004-2008), P. V. Sushko (Research Associate 2001-2004; Senior Research Associate 2005-2009; Lecturer 2009-2012; Reader 2012-present) and K. P. McKenna (Research Associate 2005-2009; Senior Research Associate 2009-2011).

This research was funded by the EU FP6 programme, EPSRC and by SMT (TX, USA). It was carried out in close collaboration with SMT, the leading R&D consortium in this area, who provided the experimental data on the electrical characterisation of devices and spectroscopic defect properties. Collaboration with SMT was coordinated by Dr. G. Bersuker and Dr. B. H. Lee. Prof. A. Shluger was a visiting professor at SMT in 2009. Researchers in Dept. Enginyeria Electrònica, Universitat Autònoma de Barcelona provided the Conductive Atomic Force Microscopy measurements used in reference [5].

3. References to the research

[1] Vacancy and interstitial defects in hafnia, A. S. Foster, F. Lopez Gejo, A. L. Shluger and R. M. Nieminen, *Phys. Rev. B*, 65, 174117 (2002) doi:10.1103/PhysRevB.65.174117

[2] The role of nitrogen-related defects in high-k dielectric oxides: Density-functional studies, J. L. Gavartin, A. L. Shluger, A. S. Foster and G. I. Bersuker, *J. Appl. Phys.*, 97(5), 053704 (2005) doi:10.1063/1.1854210

[3] Negative oxygen vacancies in HfO_2 as charge traps in high-*k* stacks, J. L. Gavartin, D. Muñoz-Ramo, A. L. Shluger, G. I. Bersuker and B. H. Lee, *Appl. Phys. Lett.*, 89, 082908 (2006) doi:10.1063/1.2236466

[4] The interaction of oxygen vacancies with grain boundaries in monoclinic HfO_2, K. P. McKenna and A. L. Shluger, *Appl. Phys. Lett.*, 95, 222111 (2009) doi:10.1063/1.3271184

[5] Grain boundary mediated leakage current in polycrystalline HfO_2 films, K. P. McKenna, A. L. Shluger, V. Iglesias, M. Porti, M. Nafría, M. Lanza, and G. Bersuker, *Microel. Engineering*, 88, 1272-1275 (2011) doi:10.1016/j.mee.2011.03.024

References [1], [2] and [4] best indicate the quality of the underpinning research.

Relevant research grants:

(i) FP6 IST STREP, High K Dielectric Film Growth (HIKE), 2001-05, UCL PI: A. Shluger, UCL budget €310,000

(ii) EPSRC Materials Modelling Initiative GR/S80080/01, Meeting the materials challenges of nano-CMOS electronics (jointly with the University of Glasgow and NASA), 2004-08, PI: A. Shluger, total grant value £787,000

(iii) SEMATECH, Modelling of charge traps in high-k dielectrics, 2004-present, PI: A. Shluger, $300,000

4. Details of the impact

Knowledge transfer between UCL and industry has enabled technological developments in the microelectronics industry, including the employment of HfO_2 in new products. This has been facilitated by UCL contracts with SEMATECH (SMT), a non-profit, world-leading technology research and development consortium, which includes several of the world's biggest microchip manufacturers – IBM, Intel, TSMC, Samsung and GlobalFoundries – as full members, and over 40 other semiconductors-related companies as associated members. The consortium works to accelerate the development of the advanced manufacturing technologies that will be needed to build more powerful semiconductor devices. Contracts with research consortiums such as SMT are vital for university research groups to be able to contribute to the development of new technology and secure impact in the microelectronics industry.

Research findings from the Shluger group at UCL, along with those from many other research groups, are collated by SMT and presented by them to their member companies on a regular basis via confidential reports. Member companies then make use of these findings, together with their own in-house research, to enable technological developments and new devices such as improved transistors. Due to the highly confidential nature of this industry it is impossible to deduce which particular research findings are implemented by the member companies in their improved devices; however, the fact that UCL research has been continuously financially supported by the industry (via its research consortium) since 2004 constitutes an unambiguous proof of its practical significance. The UCL results and analysis - and process modifications based on these results – contained in SMT's confidential reports have also been consistently highly evaluated by the member companies [A]. Industry's high valuation of the research presented to it by SMT, including that from UCL, also ensures that the consortium is able to keep operating [A].

Since 2004, the Shluger group has been actively involved in three major programmes at SMT. For each of these programmes, the UCL research described in section 2 has helped SMT to meet their obligations to their member companies by providing them with important insights, which they were able to pass on. The particular impacts described below all took place after 1 January 2008 [B].

One programme was the development of the next generation of gate dielectrics, the so-called higher-k dielectrics, intended for transistor devices with an effective oxide thickness (EOT) of less than 0.5nm (required by the International Technology Roadmap for Semiconductors). Scaling the transistor size helps to increase their packing density and improve performance and power consumption of microchips. The UCL group provided an understanding of the material properties responsible for the HfO_2 dielectric constant, which enabled SMT to fabricate and demonstrate transistors with an EOT of 0.49nm [B]. The understanding of the origin and structure of defects in HfO_2 and at Si/HfO_2 interfaces developed by the Shluger group also provided the way to minimise the negative impact of these defects by modifying processing conditions; SMT confirmed that the proposal made in the UCL work to apply the post-deposition anneal using ammonia improved device transconductance and reduced device threshold voltage instability. Additionally, the UCL group's determination of the size of the electron traps enabled the thickness of the HfO_2 layer to be scaled down to below 2.5nm, drastically reducing the instability [A].

Another programme involved the development of advanced non-volatile memory, based on a well-controlled and highly repeatable change of the dielectric resistivity rather than on a conventional electron storage technology. SMT reported that: "Calculations of the sub-stoichiometric poly-crystalline dielectric structures performed by Prof. Shluger's group allowed to pinpoint that the grain boundaries are the critical morphological material properties which define the resistive switching paths. Furthermore, Prof. Shluger's study identified atomic characteristics of the oxygen vacancies at the grain boundaries and their kinetic, which played a critical role in resistive switching process. Based on these findings, SMT was able to optimize the material properties and fabricate high performance memory devices meeting the project objectives" [B]. They added that "the UCL contribution is highly valuable" for this programme [B].

The third programme involved the mechanisms of dielectric degradation, which, to a great degree,

determines overall device reliability. The UCL group's research provided an atomic-level description of the defect generation process in the SiO_2 dielectric when subjected to electrical stress. This research finding was employed by SMT to develop a model capable of estimating the device lifetime, which received high evaluation by member companies [B].

All of the important insights above were communicated by SMT to their member companies and, together with contributions from many other research groups, have enabled technological developments in the microelectronics industry, including the employment of HfO_2 in new products.

For example, in 2009, Intel released a new 32nm microchip [C] that uses the hafnium-based dielectric [A]. This was an improvement on its 45nm microchip released in 2007, which was the first technology node to use the new high-k dielectric material. To enable production of the 32nm technology, modifications were mostly made to the device architecture and sizes, improvements that were underpinned by research including that conducted by the Shluger group. For example, the EOT of the high-k dielectric was reduced from 1.0nm in the 45nm technology to 0.9nm in the 32nm technology [C]. Further technological improvements enabled Intel to release in 2011 the even smaller 22nm transistor technology [D], which also uses the hafnium-based dielectric [A]. Other companies – IBM, TSMC, Samsung and GlobalFoundries – now also make use of the hafnium-based dielectric in their microchip technologies.

5. Sources to corroborate the impact

[A] A Fellow at SEMATECH can be contacted to corroborate the impact of the UCL research on SMT, the consistent high evaluation of research findings by member companies, the impact on technological developments at SMT, and the use of the hafnium-based dielectric in Intel's 32nm and 22nm devices. Contact details provided separately.

[B] Supporting statement from a Fellow at SEMATECH – corroborates the impact of the UCL research findings on three programmes at SMT in the last five years. Available on request.

[C] *Introduction to Intel's 32nm Process Technology* http://intel.ly/19znq0g – corroborates that Intel released the 32nm process technology with second generation high-k and metal gate transistors in 2009, and corroborates the improvement in EOT.

[D] Intel's webpage about their 22nm technology http://intel.ly/1fZgH9j – corroborates the release of Intel's 22nm process technology in 2011.